CONSOLE CHIP AND ONE-BUS SYSTEM

FIELD OF THE INVENTION

[0001] This invention relates to a multi-media computer system, and more particularly to a multi-media computer system with a single bus shared by audio, video, and application programs.

BACKGROUND OF THE INVENTION

[0002] As the technology progresses rapidly, the multi-media computer system is now widely available at an affordable price to most users. Conventional multi-media computer systems are usually designed to accommodate add-on audio video functional modules, so that existing systems can be upgraded. Hence, the synchronization of many data and control buses plays an important role in determining the performance of the multi-media computer system.

[0003] FIG. 1 shows a conventional two-bus system, including a CPU/Sound/Graphic unit 1, a program and sound memory 2, a graphic memory 3, a TV/LCD signal unit 4, a program and sound bus 5, and a graphic bus 6. CPU/Sound/Graphic unit 1 communicates with program and sound memory 2 through program and sound bus 5, while with graphic memory 3 through graphic memory 6. After processed or displayed data are then to TV/LCD signal unit 4, and separated into video output, and audio outputs.

[0004] Conventional structure of two-bus multi-media computer systems have several shortcomings to having two buses. As the CPU/Sound/Graphic unit 1 can only communicate with a memory at one time, the two buses must be synchronized in communicating with CPU/Sound/Graphic unit 1. The synchronization adds extra overhead to CPU/Sound Graphic unit 1 and wastes precious processing cycles. Further more, the circuit complexity of CPU/Sound/Graphic unit 1 increase because it also need extra circuit to perform the synchronization.

SUMMARY OF THE INVENTION

[0005] The object of the present invention is to provide a one-bus computer system so that the CPU performance can be improved by avoid wasting precious CPU cycles on bus synchronization, and waiting for slow memory speed.

[0006] Another object of the present invention is to provide a one-bus computer system so that the circuit complexity of CPU can be reduced due to the elimination of bus synchronization task, which, in turn, will reduce the number of the pin number required.

[0007] Yet another object of the present invention is to provide a bus-arbitration device which is capable of performing bus arbitration among a plurality of buses so that design and routing of multiple-bus computer systems can be simplified.

[0008] To achieve the aforementioned objects, the present invention adopts ASIC technology to provide a bus-arbitrator chip and redesign a novel architecture of a

computer system. In the present invention, the program and sound memory and the graphic memory of FIG. 1 are consolidated into a program and sound and graphic memory, which communicates with the CPU/Sound/Graphic unit through a bus arbitrator with a single bus. The addition of the bus-arbitrator can relieve the CPU/Sound/Graphic unit from performing bus synchronization and waiting for the slow memory to catch up.

[0009] These and other objects, features and advantages of the invention will be apparent to those skilled in the art, from a reading of the following brief description of the drawings, the detailed description of the preferred embodiment, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 shows a schematic view of a conventional two-bus computer system.

[0011] FIG. 2 shows schematic view of a one-bus computer system of the present invention.

[0012] FIG. 3 shows a detailed block diagram of a one-bus computer system of the present invention.

[0013] FIG. 4 shows a block diagram of the sound unit in a system of the present invention.

[0014] FIG. 5 shows a block diagram of the bus arbitrator in a system of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] As shown in FIG. 2, the present invention of a one-bus multi-media computer system comprises a CPU/Sound/Graphic unit 21 connected to a program and sound bus 25 and a graphic bus 26, a bus arbitrator 22 connected to program and sound bus 25 and graphic bus 26 on one side, and one-bus 27 on the other side, a program and sound and graphic memory 23 connected to one-bus 27, and a TV/LCD signal unit 24 for outputting audio and video signals. CPU/Sound/Graphic unit 21 requests said program and sound and graphic memory 23 by memory addresses, processes data returned from program and sound and graphic memory 23, and sends the signals to TV/LCD signal unit 24 for outputting. Bus arbitrator 22 sits between CPU/Sound/Graphic 21 and program and sound and graphic memory 23 to arbitrate the memory requests from CPU/Sound/Graphic unit 21 to program and sound and graphic memory 23. Program and sound memory 12 and graphic memory 13 of FIG. 1 are consolidated into a program and sound and graphic memory 23, which communicates with CPU/Sound/Graphic unit 21 through a bus arbitrator 22 with a single bus 27. The addition of bus-arbitrator 22 can relieve CPU/Sound/Graphic unit 21 from performing bus synchronization and waiting for the slow memory to catch up.

[0016] FIG. 3 shows a detailed block diagram of a computer system of the present invention. As shown in FIG. 3, the system includes a CPU 32, a sound unit 33, a graphic unit 34, and internal program memory 31, an internal video memory 35, a bus-arbitrator 22, and an external memory 37. Internal program memory 31 receives a memory request address from address bus 31a and exchanges the data for that memory address with CPU 32 through data bus 31b. CPU 32 also sends CPU address ports information 32a to sound unit 33, and relays PCU address ports information 33a

to graphic unit 34. All CPU 32, sound unit 33, and graphic unit 34 send memory request addresses to bus arbitrator 22 through address buses 32b, 33b, and 34c, respectively. The data are exchanged from and to bus arbitrator 22 through data buses 32c, 33c, and 34d, respectively. An additional address bus 34a and data bus 34b are used by graphic unit 34 to communicate with internal video memory 35. Bus arbitrator 22 communicates with an external memory 37 through an address bus 36a and a data bus 36b. The output outputs from sound unit 33 are audio1 and audio2 streams, and graphic unit 34 outputs video stream.

[0017] Basically, bus arbitrator 22 arbitrates the bus accessibility with the rule that a memory request to a faster memory is given a higher priority to access the bus without the pre-emptive capability. Hence, when the bus is available and two or more memories request to use the bus, the request to the memory having the fastest speed is given the highest priority, and the others will wait unit their respective turn to access the memory. On the other hand, when the bus is unavailable and two or more memories request to use the bus, all the requests for the bus accessing are given a priority based on their memory speed, and wait unit their respective turn. The memory currently accessing the bus will finish the use of bus regardless of its memory speed.

[0018] FIG. 4 shows a block diagram of the sound unit of the system of the present invention. As shown in FIG. 4, the sound unit includes four rhythm channels 42, 43, 44, 45, two low frequency channels 46, 47, two noise channels 48, 49, a built-in DM 50, and a built-in PCM 51. CPU address ports 41 is to provide signals for controlling

the operation of the sound unit. The sound unit also includes two independent outputs a first audio and a second audio.

[0019] FIG. 5 shows a block diagram of the bus arbitrator of the present invention. As shown in FIG. 5, the bus arbitrator includes an address bus multiplexer 61 and a first data register 62. Address bus multiplexer 61 takes two inputs, a first bus address 61a and a second bus address 61b, and multiplex to generate an output, one-bus address61c. In the embodiment, the first bus 61a is a low frequency program and sound system bus, and the second bus 61b is a high frequency video bus. The data from one-bus, called one-bus data 62c, can be either temporarily stored in the first data register 62 or directly outputted to a second data bus. The operation of address bus multiplexer 61 and the first data register 62 is controlled by a bus control signal, second bus signal OEB. When the second bus signal OEB is low, the address bus multiplexer takes the second bus address 61b and outputs one-bus address61c. At the same time, the first data register 62 stores the one-bus data 62c and outputs a first bus data 62a. On the other hand, when the second bus signal OEB is high, it is the accessing cycle for the first bus untill the second bus signal OEB becomes low. During the accessing cycle of the first bus, one-bus data is transported to the first bus data. The video system gets a second bus data 62b before the second bus signal OEB transits from low to high.

[0020] While the invention has been described in connection with what is presently considered to the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but, on the contrary, it should be clear to those skilled in the art that the description of the embodiment is

intended to cover various modifications and equivalent arrangement included within the spirit and scope of the appended claims.